

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR U.S. LETTERS PATENT

Title:

**SELF-ALIGNED MRAM CONTACT AND METHOD OF  
FABRICATION**

Inventor:

**Roger Lee**

Dickstein Shapiro Morin & Oshinsky LLP  
2101 L Street NW  
Washington, DC 20037-1526  
(202) 785-9700

0305044 034504  
0305044 034504

## SELF-ALIGNED MRAM CONTACT AND METHOD OF FABRICATION

## FIELD OF THE INVENTION

[0001] The present invention relates MRAM semiconductor structures and, more particularly, to a method of forming self-aligned contacts in MRAM structures.

## BACKGROUND OF THE INVENTION

[0002] Magnetic random access memories (MRAMs) employ magnetic multilayer films as storage elements. When in use, an MRAM cell stores information as digital bits, which in turn depend on the alternative states of magnetization of thin magnetic multilayer films forming each memory cell. As such, the MRAM cell has two stable magnetic configurations, high resistance representing a logic state 0 and low resistance representing a logic state 1, or vice versa.

[0003] A typical multilayer-film MRAM includes a number of bit or digit lines intersected by a number of word lines. At each intersection, a film of a magnetically coercive material is interposed between the corresponding bit line and word line. Thus, this magnetic material and the multilayer films from the digit lines form a magnetic memory cell which stores a bit of information.

[0004] The basic memory element of an MRAM is a patterned structure of a multilayer material, which is typically composed of a stack of different

materials, such as copper (Cu), tantalum (Ta), permalloy (NiFe) or aluminum oxide ( $\text{Al}_2\text{O}_3$ ), among others. The stack may contain as many as ten different overlapping material layers and the layer sequence may repeat up to ten times. Fabrication of such stacks requires deposition of the thin magnetic materials layer by layer, according to a predefined order.

[0005] Figure 1 shows an exemplary conventional MRAM structure including MRAM stacks 22 which have three respective associated bit or digit lines 18. The digit lines 18, typically formed of copper (Cu), are first formed in an insulating layer 16 formed over underlayers 14 of an integrated circuit (IC) substrate 10. Underlayers 14 may include, for example, portions of integrated circuitry, such as CMOS circuitry. A pinned layer 20, typically formed of ferromagnetic materials, is provided over each digit line 18. A pinned layer is called "pinned" because its magnetization direction does not rotate in the presence of applied magnetic fields.

[0006] Many attempts are currently being made to integrate structures of magnetic random access memories, such as the MRAM stack 22 of Figure 1, with semiconductor devices, for example CMOS circuits and/or with circuitry that can be formed over such integrated MRAM/CMOS devices. For this, conventional small contact openings from the pinned layers 20 of Figure 1, for example, to word line conductors (not shown) are typically formed by photolithography techniques.

[0007] As known in the art, the photolithography techniques employ a mask that must be previously aligned to define small openings in such MRAM structures. With increased packing density of MRAM cells, however, there is a need for minimizing if not eliminating mask misalignment problems posed by the conventional photolithography techniques when forming small contact openings from MRAM stacks to adjacent circuitry. Accordingly, there is a need for an improved method for fabricating high quality MRAM structures, such as pinned layers and digit lines, which are highly integrated with a CMOS circuit, and which have self-aligned contacts that minimize the misalignment drawbacks of the prior art.

#### SUMMARY OF THE INVENTION

[0008] The present invention provides a method for forming self-aligned MRAM contacts for MRAM structures, such as magnetic layers of an MRAM stack, formed over various underlayers of an integrated circuit substrate. In an exemplary embodiment of the invention, MRAM stacks are formed to include a top layer of a conductive material, such as tungsten nitrogen. An insulating material is formed over the whole substrate including the MRAM stacks. The insulating material is subsequently chemically mechanically polished (CMP) to expose the upper surface of such conductive material and to form a self-aligned MRAM contact on a respective MRAM stack. Subsequent word lines and conductive plugs are formed over the self-aligned MRAM contacts.

[0009] These and other features and advantages of the invention will be more apparent from the following detailed description which is provided in connection with the accompanying drawings, which illustrate exemplary embodiments of the invention.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Figure 1 is a schematic three-dimensional view of a portion of a conventional MRAM structure.

[0011] Figure 2 illustrates a partial cross-sectional view of a semiconductor topography, at an intermediate stage of the processing, wherein a self-aligned MRAM contact will be constructed in accordance with the present invention.

[0012] Figure 3 illustrates a partial cross-sectional view of the self-aligned MRAM contact of the present invention at a stage of processing subsequent to that shown in Figure 2.

[0013] Figure 4 illustrates a partial cross-sectional view of the self-aligned MRAM contact of the present invention at a stage of processing subsequent to that shown in Figure 3.

[0014] Figure 5 illustrates a partial cross-sectional view of the self-aligned MRAM contact of the present invention at a stage of processing subsequent to that shown in Figure 4.

[0015] Figure 6 illustrates a partial cross-sectional view of the self-aligned MRAM contact of the present invention at a stage of processing subsequent to that shown in Figure 5.

[0016] Figure 7 illustrates a partial cross-sectional view of the self-aligned MRAM contact of the present invention at a stage of processing subsequent to that shown in Figure 6.

[0017] Figure 8 illustrates a partial cross-sectional view of the self-aligned MRAM contact of the present invention at a stage of processing subsequent to that shown in Figure 7.

[0018] Figure 9 illustrates a partial cross-sectional view of the self-aligned MRAM contact of the present invention at a stage of processing subsequent to that shown in Figure 8.

[0019] Figure 10 illustrates a partial cross-sectional view of the self-aligned MRAM contact of the present invention at a stage of processing subsequent to that shown in Figure 9.

[0020] Figure 11 illustrates a partial cross-sectional view of the self-aligned MRAM contact of the present invention at a stage of processing subsequent to that shown in Figure 10.

[0021] Figure 12 illustrates a partial cross-sectional view of the self-aligned MRAM contact of the present invention at a stage of processing subsequent to that shown in Figure 11.

[0022] Figure 13 illustrates a partial cross-sectional view of the self-aligned MRAM contact of the present invention at a stage of processing subsequent to that shown in Figure 12.

[0023] Figure 14 illustrates a partial cross-sectional view of the self-aligned MRAM contact of the present invention at a stage of processing subsequent to that shown in Figure 13.

[0024] Figure 15 illustrates a partial cross-sectional view of the self-aligned MRAM contact of the present invention at a stage of processing subsequent to that shown in Figure 14.

[0025] Figure 16 is a partial three-dimensional view of the self-aligned MRAM contact of Figure 15 at a stage of processing subsequent to that shown in Figure 15.

[0026] Figure 17 is a partial three-dimensional view of the self-aligned MRAM contact of Figure 15 at a stage of processing subsequent to that shown in Figure 16.

[0027] Figure 18 is a partial three-dimensional view of the self-aligned MRAM contact of Figure 15 at a stage of processing subsequent to that shown in Figure 17.

[0028] Figure 19 is a partial three-dimensional view of the self-aligned MRAM contact of Figure 15 at a stage of processing subsequent to that shown in Figure 18.

[0029] Figure 20 is a schematic diagram of a processor system incorporating the self-aligned MRAM contact constructed in accordance with the present invention.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0030] In the following detailed description, reference is made to various exemplary embodiments of the invention. These embodiments are described with sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be employed, and that structural and electrical changes may be made without departing from the spirit or scope of the present invention.

[0031] The term "substrate" used in the following description may include any semiconductor-based structure that has an exposed semiconductor surface. Structure must be understood to include silicon, silicon-on insulator (SOI), silicon-on sapphire (SOS), doped and undoped semiconductors, epitaxial



layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. The semiconductor need not be silicon-based. The semiconductor could be silicon-germanium, germanium, or gallium arsenide. When reference is made to substrate in the following description, previous process steps may have been utilized to form regions or junctions in or on the base semiconductor or foundation.

[0032] The term "metal" is intended to include not only elemental metal, but metal with other trace metals or in various alloyed combinations with other metals as known in the semiconductor art. The term "metal" is also intended to include conductive oxides of such metals, as well as doped semiconductors and their respective conductive oxides.

[0033] Referring now to the drawings, where like elements are designated by like reference numerals, Figures 2-19 illustrate an exemplary embodiment of a method of forming self-aligned MRAM contacts (Figures 18-19) in MRAM structures. Figure 2 depicts a portion of a semiconductor substrate 50 on which underlying layer 52 has been already formed according to well-known methods of the prior art. The underlying layer 52 could include, for example, circuit layers forming CMOS devices and circuits.

[0034] Referring now to Figure 3, an insulating layer 54 is formed over the substrate 50 and the underlying layer 52. In an exemplary embodiment of the invention, the insulating layer 54 is blanket deposited by spin coating to a

00005914-031501  
FILED IN 00-0327

thickness of about 1,000 Angstroms to about 10,000 Angstroms. However, other known deposition methods, such as sputtering by chemical vapor deposition (CVD), plasma enhanced CVD (PECVD), or physical vapor deposition (PVD), may be used also in accordance with the characteristics of the IC device already formed. The insulating layer 54 may be formed of a conventional insulator, for example, a thermal oxide of silicon, such as SiO or SiO<sub>2</sub>, or a nitride such as Si<sub>3</sub>N<sub>4</sub>. Alternatively, a high temperature polymer, such as a polyimide, or a low dielectric constant inorganic material may also be employed.

[0035] Next, as illustrated in Figure 4, a photoresist layer 55 is formed over the insulating layer 54. The photoresist layer 55 is exposed through a mask 56 (Figure 5) with high-intensity UV light. The mask 56 may include any suitable pattern of opaque and clear regions that may depend, for example, on the desired pattern to be formed in the insulating layer 54. This way, portions 55a of the photoresist layer 55 are exposed through portions 56a of the mask 56 wherever portions of the insulating layer 54 need to be removed.

[0036] Although Figure 5 schematically illustrates mask 56 positioned over the photoresist layer 55, those skilled in the art will appreciate that mask 56 is typically spaced from the photoresist layer 55 and light passing through mask 56 is focussed onto the photoresist layer 55. After exposure and development of the exposed portions 55a, portions 55b of the unexposed and undeveloped photoresist are left over the insulating layer 54, as shown in Figure 6. This way, openings 57 (Figure 6) are formed in the photoresist layer 55.

[0037] An etch step is next performed to obtain grooves 58 in the insulating layer 54, as illustrated in Figures 7-8. The grooves 58 are etched to a depth of about 500 Angstroms to about 2,000 Angstroms, more preferably of about 1,000 Angstroms. Subsequent to the formation of the grooves 58, the remaining portions 55b of the positive photoresist layer 55 are then removed by chemicals, such as hot acetone or methylethylketone, or by flooding the substrate 50 with UV irradiation to degrade the remaining portions 55b to obtain the structure of Figure 8.

[0038] Subsequent to the formation of the grooves 58 (Figures 7-8), a thin barrier layer 59 is formed in the grooves 58 and over the insulating layer 54, and then chemical mechanical polished to remove barrier layer material from the top portions of the insulating layer 54, as shown in Figure 9. The barrier layer 59 may comprise bonding materials such as tantalum (Ta), titanium (Ti), titanium-tungsten (TiW), titanium nitride (TiN) or chromium (Cr), among others. The barrier layer 59 forms a strong mechanical and chemical bond between the conductive material which will be formed later and the insulating layer 54 to help prevent peeling of the formed conductive layer from the insulating layer. In a preferred embodiment of the invention, the barrier layer 59 is formed of sputtered tantalum. In this embodiment, tantalum is deposited to a thickness of about 5nm to about 10nm.

[0039] Next, as illustrated in Figure 10, a conductive material layer 60 is formed over the barrier layer 59 and the insulating layer 54 to fill in the grooves

58. In a preferred embodiment, the conductive material comprises copper (Cu). However, other conductive materials such as aluminum, tungsten or gold, among others, may be used also. Further, metal alloys may be employed also, depending on desired characteristics of the IC device.

[0040] The conductive material layer 60 is formed over the barrier layer 59 by deposition, for example, and then excess material is removed to form metal lines 62 (Figure 11). In an exemplary embodiment of the present invention, the excess conductive material layer 60 is removed by means of chemical mechanical polishing (CMP) or a well-known RIE dry etching process. Either way, the top surfaces of the barrier layer 59 and the metal lines 62 are substantially flat and uniform across the entire surface of the substrate, as shown in Figure 11. Each metal line 62 will form the bit or digit line of a conventional MRAM structure.

[0041] After the CMP polishing process, the processing steps for the completion of the MRAM structures 100 having self-aligned MRAM contacts 99 (Figures 18-19) are now carried out. As such, a plurality of magnetic multilayer films constituting a first magnetic member 79 are first formed over the metal lines 62, which will be later patterned into pinned layers 91 (Figure 16). The first magnetic member 79 is formed of various material layers, described below in more detail, which are successively deposited over the metal lines 62 and the insulating layer 54, as illustrated in Figure 12.

Patented by Micron Technology, Inc.

[0042] In an exemplary embodiment of the present invention and as illustrated in Figure 12, a first tantalum (Ta) layer 71 (of about 20-400 Angstroms thick, more preferably of about 50 Angstroms thick), a first nickel-iron (NiFe) layer 73 (of about 10-100 Angstroms thick, more preferably of about 60 Angstroms thick), a manganese-iron (MnFe) layer 75 (of about 10-100 Angstroms thick, more preferably of about 100 Angstroms thick) and a second nickel-iron (NiFe) layer 77 (of about 10-100 Angstroms thick, more preferably of about 60 Angstroms thick) are successively blanket deposited over the insulating layer 54 and the metal lines 62, to form the first magnetic member 79. Deposition of the layers 71, 73, 75 and 77 may be accomplished by magnetron sputtering, for example. However, other conventional deposition methods may be used also, as desired.

[0043] Following the deposition of the layers 71, 73, 75 and 77, a nonmagnetic, electrically nonconductive layer 80 formed of, for example, aluminum oxide ( $\text{Al}_2\text{O}_3$ ) (of about 5-25 Angstroms thick, more preferably of about 15 Angstroms thick) is next formed overlying the first magnetic member 79, as shown in Figure 13. Although aluminum oxide is the preferred material, it must be understood that the invention is not limited to its use, and other non-magnetic materials, such as copper (Cu), titanium oxide ( $\text{TiO}_2$ ), magnesium oxide ( $\text{MgO}$ ), silicon oxide ( $\text{SiO}_2$ ) or aluminum nitride (AlN), may be used also.

[0044] Referring now to Figure 14, a plurality of magnetic multilayer films forming a second magnetic member 89 are next formed over the

nonmagnetic layer 80. Accordingly, in an exemplary embodiment of the present invention, a third nickel-iron (NiFe) layer 81 (of about 10-100 Angstroms thick, more preferably of about 40 Angstroms thick), a second tantalum (Ta) layer 83 (of about 10-100 Angstroms thick, more preferably of about 50 Angstroms thick) and a conductive layer 85 (of about 100-400 Angstroms thick, more preferably of about 200-300 Angstroms thick) are successively blanket deposited over the nonmagnetic layer 80, to form the second magnetic member 89, as shown in Figure 14. Deposition of the layers 81, 83 and 85 may be accomplished by magnetron sputtering, for example, but other conventional deposition methods may be used also, depending on the characteristics of the IC devices constructed previously to the formation of the MRAM structures 100 (Figure 19).

[0045] In an exemplary embodiment of the present invention, the conductive layer 85 may be formed of tungsten nitrogen (WN), which is deposited to a thickness of about 100-400 Angstroms, more preferably of about 200-300 Angstroms. However, the invention is not limited to this exemplary embodiment, and other conductive materials, for example metals such as tungsten (W), copper (Cu), gold (Au) or platinum (Pt), among others, may be used also, as desired.

[0046] Next, layers 71, 73, 75, 77, 80, 81, 83 and 85 (Figures 12-14) are patterned into a plurality of MRAM structures or cells 100 (Figures 15-16) including columns of pinned layers 91 and rows of sense layers 92. Thus, each MRAM structure 100 includes the pinned layer 91 (as part of the first magnetic member 79) separated from a sense layer 92 (as part of the second magnetic

member 89) by the nonmagnetic layer 80. For simplicity, the multilayer stack forming the pinned layer 91 is illustrated in Figure 16 as a single layer. Similarly, the multilayer stack forming the sense layer 92 is also illustrated in Figure 16 as a single layer. It must be understood, however, that the pinned layer 91 includes portions of the copper line 62 and of the layers 71, 73, 75 and 77, while the sense layer 92 includes portions of the layers 81, 83 and 85.

[0047]        Patterning of the plurality of layers forming the pinned and sense layers of the MRAM structures 100 (Figure 16), that is patterning of layers 71, 73, 75, 77, 80, 81, 83 and 85 may be accomplished by ion milling which typically involves physical sputtering of each layer by an argon ion beam. Patterning may be also accomplished by using a reactive plasma etch, performed, for example, in electron cyclotron resonance (ECR) or other high density plasmas, such as an inductively coupled plasma system, or a helicon plasma system containing chlorine as the source gas. A mixture of chlorine with other gases, such as argon, neon or helium, among others, may be used also. In any event, the pinned and sense layers 91, 92 are patterned and etched so that the pinned layers 91 correspond to the metal lines 62 that form the bottom electrodes of the pinned layers 91.

[0048]        Next, an insulating layer 95 (Figure 17) is formed overlying the substrate 50 including the MRAM structures 100 to a thickness of about 90-10,000 Angstroms, more preferably of about 5,000 Angstroms. The insulating layer 95 completely fills the spaces between any adjacent MRAM structures 100, as shown in Figure 17. In an exemplary embodiment of the invention, the insulating

layer 95 is formed of a nitride material such as silicon nitride ( $\text{Si}_3\text{N}_4$ ), which may be formed by conventional deposition methods, such as sputtering by chemical vapor deposition (CVD), plasma enhanced CVD (PECVD), or physical vapor deposition (PVD), among others. However, other conventional insulating materials, for example, aluminum oxide, a thermal oxide of silicon, such as  $\text{SiO}$  or  $\text{SiO}_2$ , or a high temperature polymer, such as a polyimide, a low dielectric constant inorganic material, amorphous dielectric, or bias sputtered quartz may also be employed.

[0049] Subsequent to the formation of the insulating layer 95 (Figure 17), portions of the insulating layer 95 that are formed over the top surface of the MRAM structures 100 are removed by means of chemical mechanical polishing (CMP) or well-known RIE dry etching processes. In an exemplary embodiment of the invention, the insulating layer 95 is chemical mechanical polished so that an abrasive polish removes the top surface of the insulating layer 95 above the MRAM structures 100, down to or near the planar surface of the top surface of the conductive layer 85, to form respective self-aligned MRAM contacts 99 in a polished insulating layer 96, as illustrated in Figure 18. This way, the conductive layer 85, which was formed as part of the sense layer 92 of the MRAM structure 100, acts as a polishing stop layer in the formation of the self-aligned contacts 99.

[0050] Additional steps to create a functional MRAM cell having a self-aligned contact may be carried out. Thus, additional insulating layers and conductive plugs from the self-aligned MRAM contacts 99 to word line conductors, to enable bidirectional current flow in the presence of a read and write

1256863 v1: QXSV011.DOC



signal, may be formed to complete the fabrication process of such MRAM structures. For example, Figure 19 illustrates schematically three MRAM cell structures 100 coupled to a word line 93 that intersects three pinned layers 91 and associated sense layers 92 at respective self-aligned MRAM contacts 99. As known in the art, the word line 93 may be formed of copper, for example, by patterning a mask on a dielectric layer, which is formed over the sense layers 92 including the self-aligned MRAM contacts 99, and by forming a trench in which conductive word line 93 is formed on a direction orthogonal to that of the sense layer 92. For a better understanding of the invention, the polished insulating layer 96 has been omitted in Figure 19 to illustrate the pinned layers and sense layers 91, 92 below the word line 93. However, it must be understood that the space between the pinned layers and sense layers 91, 92 and below the word line 93 is filled with the insulating layer 96.

[0051] Although Figure 19 illustrates self-aligned MRAM contacts 99 in direct contact and adjacent to the word line 93, it must be understood that the invention is not limited to this embodiment, and other interceding structures, such as conductive plugs and/or metal lines from the self-aligned MRAM contacts 99 to the word line 93 may be formed also, as desired.

[0052] A typical processor based system 400 which includes a memory circuit 448, for example an MRAM with MRAM cell structures 100 having self-aligned MRAM contacts 99 (Figures 18-19) constructed according to the present invention is illustrated in Figure 20. A processor system, such as a computer

system, generally comprises a central processing unit (CPU) 444, such as a microprocessor, a digital signal processor, or other programmable digital logic devices, which communicates with an input/output (I/O) device 446 over a bus 452. The memory 448 communicates with the system over bus 452.

[0053] In the case of a computer system, the processor system may include peripheral devices such as a floppy disk drive 454 and a compact disk (CD) ROM drive 456 which also communicate with CPU 444 over the bus 452. Memory 448 may be combined with the processor, i.e. CPU 444, in a single integrated circuit.

[0054] Although the exemplary embodiments described above illustrate the formation of three MRAM cell structures 100 having respective self-aligned MRAM contacts 99 (Figures 18-19) it is to be understood that the present invention contemplates the use of a plurality of self-aligned MRAM contacts 99 of pinned layers and sense layers as part of a plurality of MRAM cells arranged, for example, in rows and columns in a memory cell array. In addition, although the exemplary embodiments described above refer to a specific topography of the MRAM structures with specific magnetic materials forming such structures, it must be understood that the invention is not limited to the above-mentioned magnetic materials, and other magnetic and ferromagnetic materials, such as nickel-iron (Permalloy) or iron, among others, may be used also. Further, although the exemplary embodiments described above refer to patterning of the MRAM

